4.5-V TO 16-V INPUT VOLTAGE, 2-A/3-A OUTPUT CURRENT, DUAL SYNCHRONOUS STEP-DOWN REGULATOR WITH INTEGRATED MOSFET

Check for Samples: TPS65270

FEATURES

- **Wide Input Supply Voltage Range (4.5 V - 16 V)**
- **0.8 V, ±1% Accuracy Reference**
- **Up to 2-A (Buck 1) and 3-A (Buck 2) Maximum Continuous Output Loading Current**
- **Low Power Pulse Skipping Mode to Achieve High Light Load Efficiency**
- **Adjustable Switching Frequency 300 kHz - 1.4 MHz Set by External Resistor**
- **Dedicated Enable and Soft-Start for Each Buck**
- **Peak Current-Mode Control with Simple Compensation Circuit**
- **Cycle-by-Cycle Over Current Protection**
- **180° Out-of-Phase Operation to Reduce Input Capacitance and Power Supply Induced Noise**
- **Available in 24-Lead Thermally Enhanced HTSSOP (PWP) and QFN 4-mm x 4-mm (RGE) (Preview Only) Packages**

APPLICATIONS

- **DTV**
- **DSL Modems**
- **Cable Modems**
- **Set Top Boxes**
- **Car DVD Players**
- **Home Gateway and Access Point Networks**
- **Wireless Routers**

DESCRIPTION/ORDERING INFORMATION

The TPS65270 is a monolithic dual synchronous buck regulator with wide operating input voltage that can operate in 5-, 9-, 12- or 15-V bus voltages and battery chemistries. The converters are designed to simplify its application while giving the designer the option to optimize their usage according to the target application.

The TPS65270 features a precision 0.8-V reference and can produce output voltages up to 15 V. Each converter features enable pin that allows dedicated control each channel that provide flexibility for power sequencing. Soft-start time in each channel can be adjustable by choosing different external capacitors.

Constant frequency peak current mode control simplifies the compensation and provides fast transient response. Cycle-by-Cycle over current protection and hiccup mode operation limit MOSFET power dissipation in short circuit or over loading fault conditions. Low side reverse current protection also prevents excessive sinking current from damaging the converter.

The switching frequency of the converters can be set from 300 KHz to 1.4 MHz with an external resistor. Two converters have clock signal with 180° out-of-phase so as to minimize the input filter requirements and alleviate EMI and input capacitor requirements.

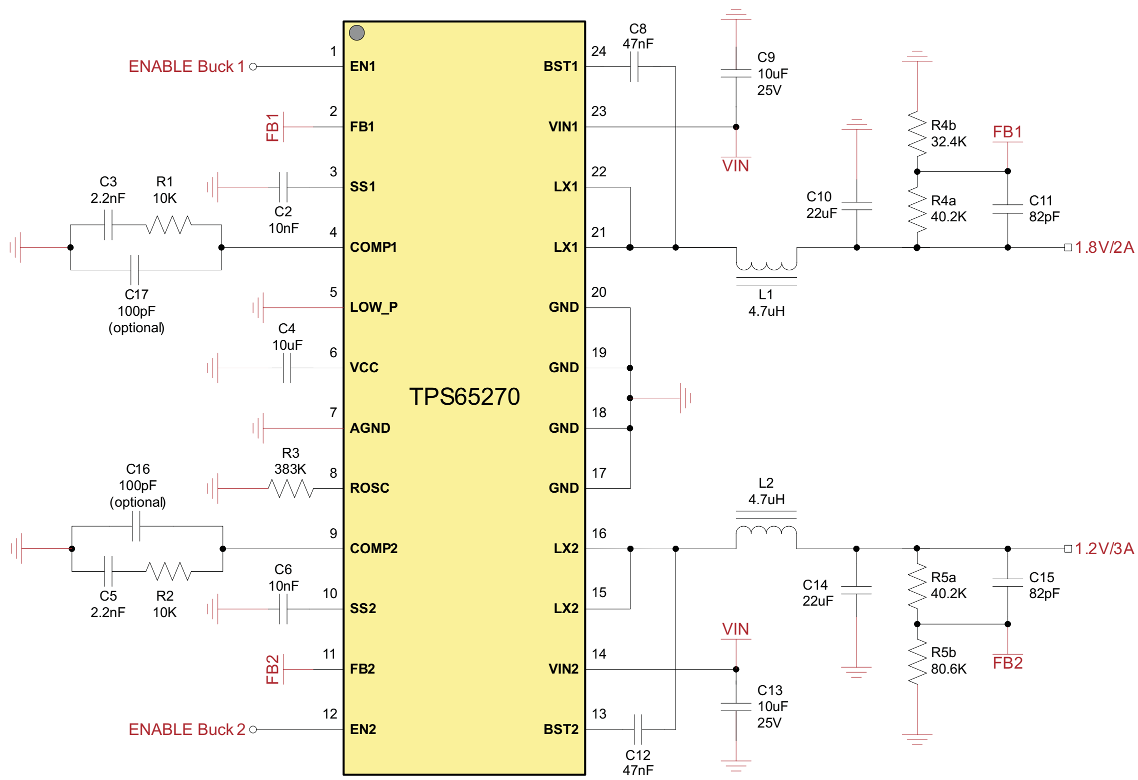
TPS65270 also features a light load pulse skipping mode (PSM). The PSM mode allows a power loss reduction on the input power supplied to the system at light loading in order to achieve light load high efficiency.

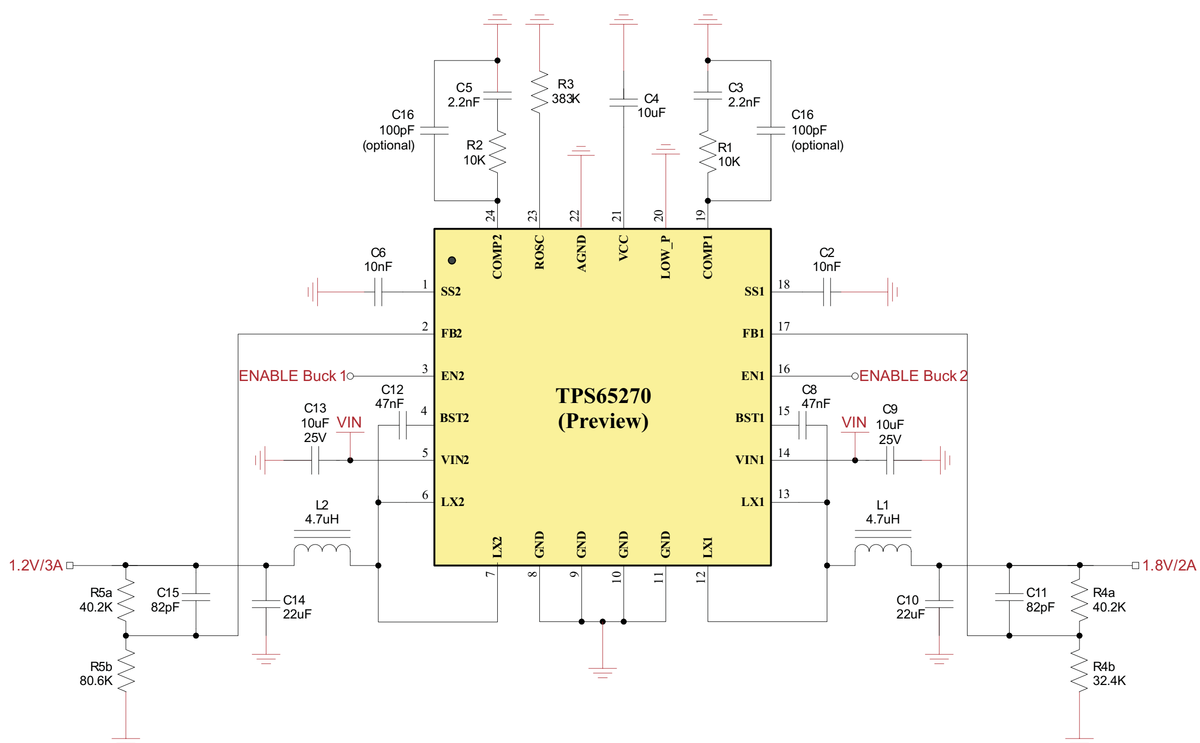
The TPS65270 is available in a 24-Lead thermally enhanced HTSSOP (PWP) package and 24-pin QFN 4-mm x 4-mm (RGE) package (preview).

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

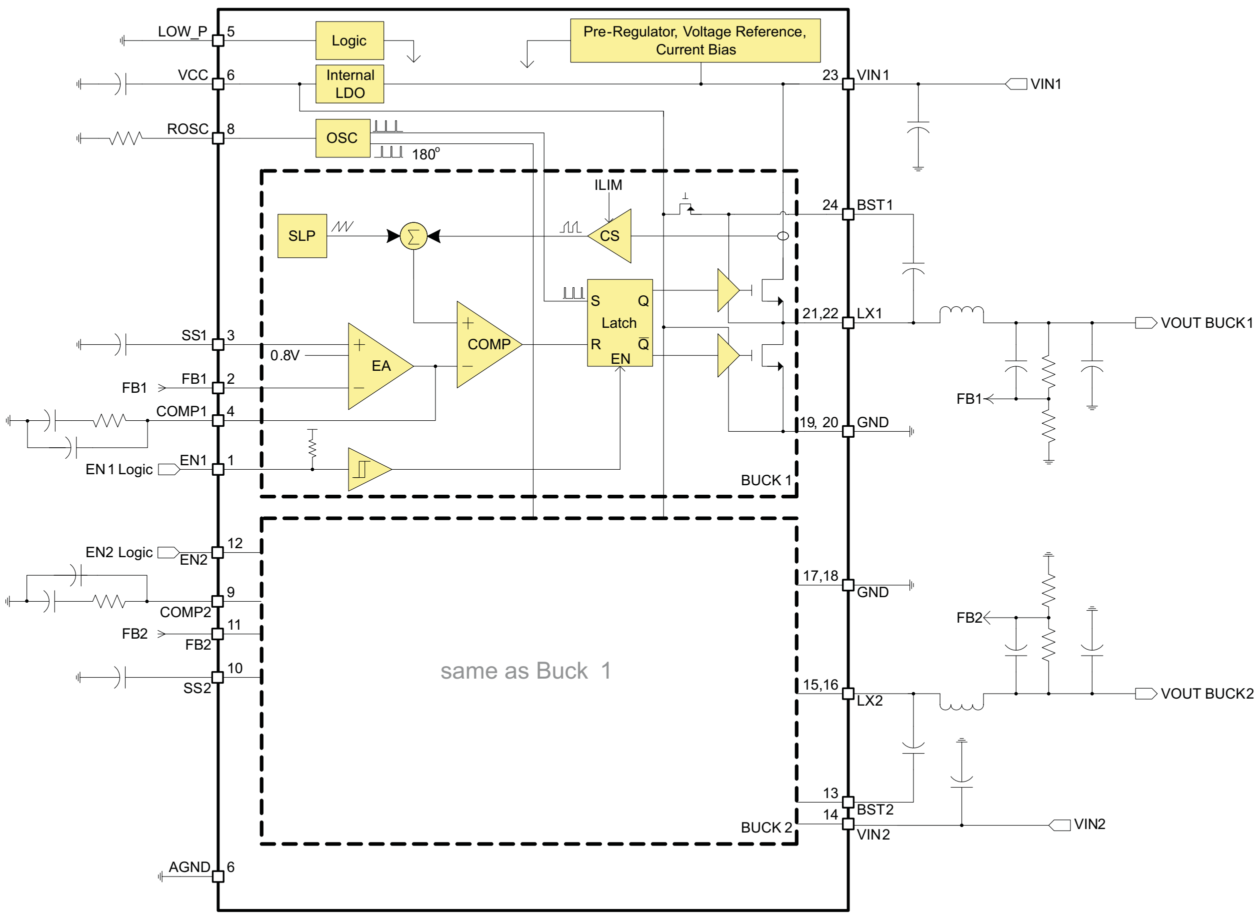
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

TYPICAL APPLICATION





FUNCTIONAL BLOCK DIAGRAM



Note: Pin numbers in block diagram are for HTSSOP (PWP) 24-pin package.

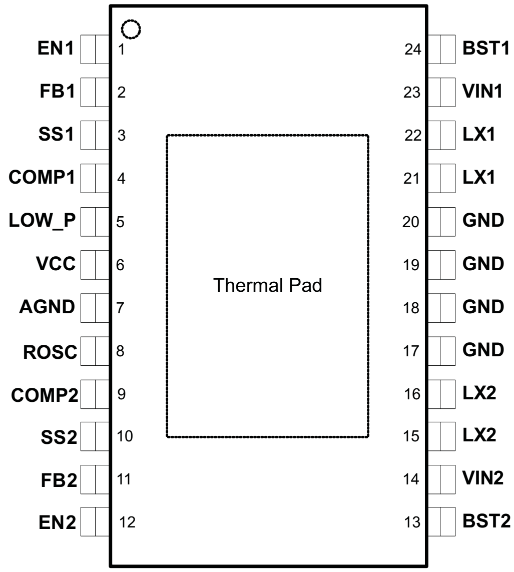
ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PWP (R-PDSO-G)	TPS65270PWPR	TPS65270
	RGE (S-PVQFN-N24) - Preview Only	TPS65270RGER or TPS65270RGET	TPS65270

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

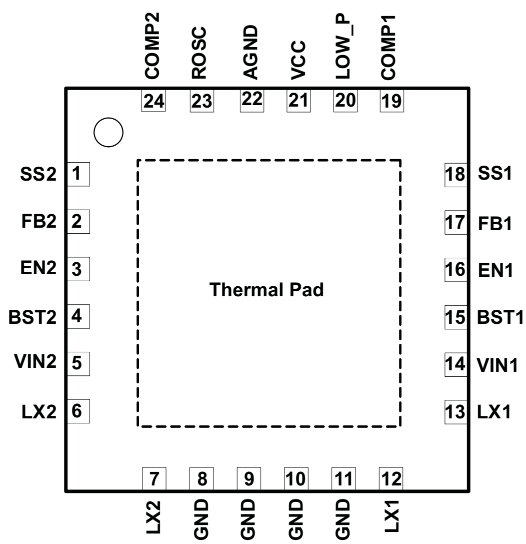
PIN OUT

PWP PACKAGE
(TOP VIEW)



Exposed pad must be soldered to PCB for optimal thermal performance.

RGE PACKAGE (PREVIEW)
(TOP VIEW)



Exposed pad must be soldered to PCB for optimal thermal performance.

TERMINAL FUNCTIONS

NAME	NO. (HTSSOP)	NO. (QFN)	DESCRIPTION
EN1	1	16	Enable for Buck 1. Logic high enables the Buck 1; Logic low disables Buck 1. If pin is left open a weak internal pull-up to V5V will allow for automatic enable; For a delayed start-up add a small ceramic capacitor from this pin to ground.
FB1	2	17	Feedback voltage for Buck 1. Connect a resistor divider to set 0.8 V from the output of the converter to ground.
SS1	3	18	Soft start input for Buck 1. An internal 5-μA charging current is sourcing to this pin. Connect a small ceramic capacitor to this pin to set the Buck 1 soft start time.
COMP1	4	19	Loop compensation pin for Buck 1. Connect a series RC circuit to this pin to compensate the control loop of this converter.
LOW_P	5	20	Low power operation mode. With active high, Buck 1 and Buck 2 operate at pulse skipping mode at light load; active low forces both Buck 1 and Buck 2 to PWM mode; this pin can't be left open.
VCC	6	21	Internal 6.5-V power supply bias. Connect a 10-μF ceramic capacitor from this pin to ground.
AGND	7	22	Analog ground. Connect all GND pins and power pad together.
ROSC	8	23	Oscillator frequency setup. Connect a resistor to ground to set the frequency of internal oscillator clock.
COMP2	9	24	Loop compensation pin for Buck 2. Connect a series RC circuit to this pin to compensate the control loop of this converter.
SS2	10	1	Soft start input for Buck 2. An internal 5-μA charging current is sourcing to this pin. Connect a small ceramic capacitor to this pin to set the Buck 1 soft start time.
FB2	11	2	Feedback voltage for Buck 2. Connect a resistor divider to set 0.8 V from the output of the converter to ground.
EN2	12	3	Enable for Buck 2. Logic high enables the Buck 2. Logic low disables Buck 2. If pin is left open a weak internal pull-up to V5V will allow for automatic enable; For a delayed start-up add a small ceramic capacitor from this pin to ground.
BST2	13	4	Bootstrapped power supply to high side floating gate driver in Buck 2. Connect a 47-nF ceramic capacitor from this pin to the switching node pin LX2.
VIN2	14	5	Input supply for Buck 2. Connect a 10-μF ceramic capacitor close to this pin.
LX2	15, 16	6, 7	Switching node connecting to inductor for Buck 2.
GND	17, 18, 19, 20	8, 9, 10, 11	Power ground for Buck 1 and Buck 2.
LX1	21, 22	12, 13	Switching node connecting to inductor for Buck 1.
VIN1	23	14	Input supply for Buck 1. Conne ct a 10-μF ceramic capacitor close to this pin.
BST1	24	15	Bootstrapped power supply to high side floating gate driver in Buck 1. Connect a 47-nF ceramic capacitor from this pin to the switching node pin LX1.
Thermal Pad			Must be soldered to PCB for optimal thermal performance. Have thermal vias on the PCB to enhance power dissipation.

ABSOLUTE MAXIMUM RATINGS [1]

over operating free-air temperature range (unless otherwise noted)

	Voltage range at VIN1, VIN2, LX1, LX2	–0.3 to 16	V
	Voltage range at LX1, LX2 (maximum withstand voltage transient < 10 ns)	–1 to 16	V
	Voltage at BST1, BST2, referenced to LX1, LX2 pin	–0.3 to 7	V
	Voltage at VCC, EN1, EN2, COMP1, COMP2, LOW_P	–0.3 to 7	V
	Voltage at SS1, SS2, FB1, FB2, ROSC	–0.3 to 3.6	V
	Voltage at AGND, GND	–0.3 to 0.3	V
T_J	Operating virtual junction temperature range	–40 to 125	°C
T_{STG}	Storage temperature range	–55 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input operating voltage	4.5		16	V
T_J	Junction temperature	–40		85	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	MAX	UNIT
Human body model (HBM)	2000		V
Charge device model (CDM)	500		V

PACKAGE DISSIPATION RATINGS [1][2][3]

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)	T_A = 25°C POWER RATING (W)	T_A = 55°C POWER RATING (W)	T_A = 85°C POWER RATING (W)
PWP	32.6	10	3.07	2.15	1.23
RGE	32.6	10	3.07	2.15	1.23

(1) This assumes a JEDEC JESD 51-5 standard board with thermal vias with High K profile - See Texas Instruments application report (SLMA002) regarding thermal characteristics of the PowerPAD™ package.
(2) This assumes junction to exposed PAD.
(3) Based on JEDEC 51.5 HIGH K environment measured on a 76.2 x 114 x .6-mm board with the following layer arrangement:
(a) Top layer: 2 Oz Cu, 6.7% coverage
(b) Layer 2: 1 Oz Cu, 90% coverage
(c) Layer 3: 1 Oz Cu, 90% coverage
(d) Bottom layer: 2 Oz Cu, 20% coverage

ELECTRICAL CHARACTERISTICS

T_A = -40°C to 125°C, V_{IN} = 12 V, f_{SW} = 625 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input Voltage range	VIN1 and VIN2	4.5		16	V
IDD_{SDN}	Shutdown	EN1 = EN2 = 0 V		10		µA
IDD_{Q_nsw}	Non switching quiescent power supply current	VFB1 = VFB2 = 900 mV, LOW_P = high		1		mA
UVLO	V_{IN} under voltage lockout	Rising V_{IN}	4	4.20	4.45	V
		Falling V_{IN}	3.65	3.85	4.10	
		Hysteresis		0.35		
V_{CC}	Internal biasing supply	V_{CC} load current = 0 A, V_{IN} = 12 V		6.25		V
V_{CC_drop}	V_{CC} LDO Drop-Out Voltage	V_{IN} = 5 V, V_{CC} load current = 20 mA		180		mV
I_{VCC}	V_{CC} current limit	4.5 V < V_{IN} < 16 V		200		mA
FEEDBACK AND ERROR AMPLIFIER						
V_{FB}	Regulated feedback voltage	V_{IN} = 12 V , V_{COM}P = 1.2 V, T_J = 25°C	-1%	0.8	1%	V
		V_{IN} = 12 V, V_{COMP} = 1.2 V, T_J = -40°C to 125°C	-2%	0.8	2%	
$V_{LINEREG}$	Line regulation - DC	V_{IN} = 4.5 V to 16 V, I_{OUT} = 1 A		0.5		%/V
$V_{LOADREG}$	Load regulation - DC	I_{OUT} = 10 % - 90% $I_{OUT,MAX}$		0.4		%/A
G_{m_EA}	Error amplifier trans-conductance	-2 µA < I_{COMP} < 2 µA		130		µs
G_{m_SRC}	COMP voltage to inductor current Gm	ILX = 0.5 A		10		A/V
ENABLE, PFM MODE AND SOFT-START						
V_{EN}	EN1 and EN2 pin threshold	Rising	1.55			V
		Falling		0.4		
V_{PSM}	PSM low power mode threshold	Rising	1.55			V
		Falling		0.4		
I_{SS}	SS1 and SS2 soft-start charging current			5		µA
OSCILLATOR						
F_{SW_BK}	Switching frequency range	Set by external resistor ROSC	0.3		1.4	MHz
F_{SW}	Programmable frequency	ROSC = 250 kΩ	0.85	1	1.15	MHz
		ROSC = 500 kΩ	425	500	575	kHz
PROTECTION						
I_{LIMIT1}	Buck 1 peak inductor current limit	4.5 V < V_{IN} < 16 V		3.2		A
I_{LIMIT1_LS1}	Buck 1 low side MOSFET current limit	4.5 V < V_{IN} < 16 V		2		A
I_{LIMIT2}	Buck 2 peak inductor current limit	4.5 V < V_{IN} < 16V		4.1		A
I_{LIMIT1_LS2}	Buck 2 low side MOSFET current limit	4.5 V < V_{IN} < 16 V		2		A
MOSFET ON-RESISTANCES						
R_{dson_HS1}	On resistance of high side FET on CH1	BST1 to LX1 = 6.25 V		120		mΩ
R_{dson_LS1}	On resistance of low side FET on CH1	V_{IN} = 12 V		80		mΩ
R_{dson_HS2}	On resistance of high side FET on CH2	BST2 to LX2 = 6.25 V		95		mΩ
R_{dson_LS2}	On resistance of low side FET on CH2	V_{IN} = 12 V		50		mΩ
T_{on_min}	Minimum in time			80	120	ns
THERMAL SHUTDOWN						
T_{TRIP}	Thermal protection trip point	Rising temperature		160		°C
T_{HYST}	Thermal protection hysteresis			20		°C

TYPICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 625 kHz (unless otherwise noted)

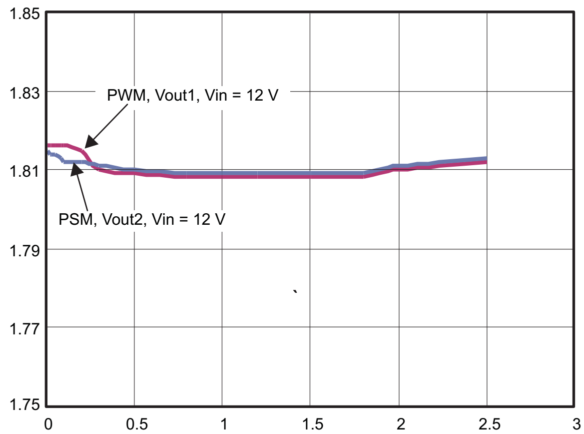


Figure 1. Load Regulation Buck 1 at 1.8 V, 1% Resistors

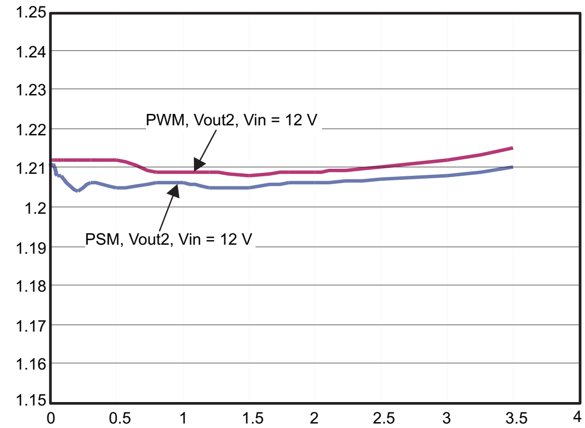


Figure 2. Load Regulation Buck 1 at 1.2 V, 1% Resistor s

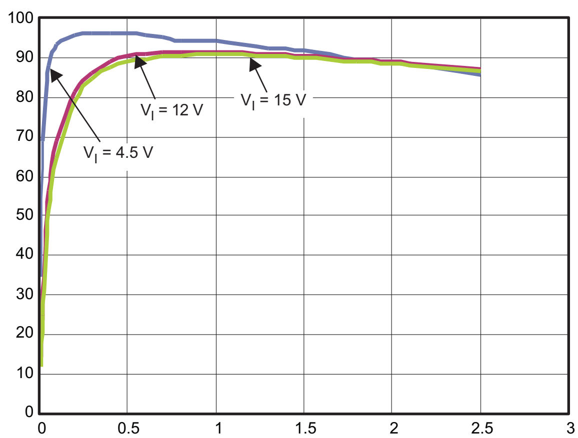


Figure 3. Efficiency Buck 1 at 3.3 V

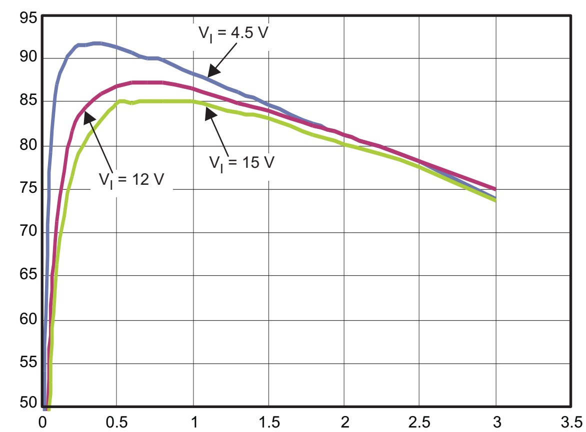


Figure 4. Efficiency Buck 2 at 1 V

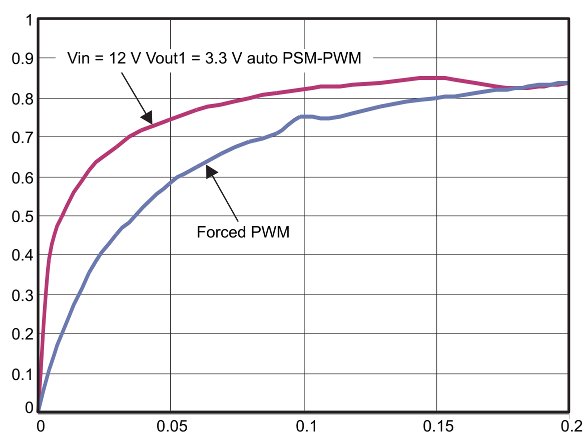


Figure 5. Efficiency Buck 1 at 3.3 V

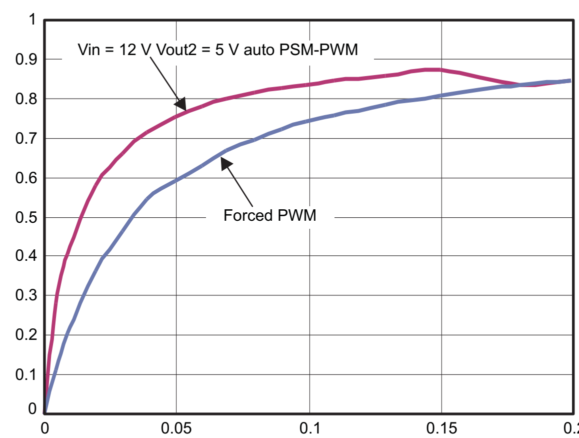


Figure 6. Efficiency Buck 2 at 5 V

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 625 kHz (unless otherwise noted)

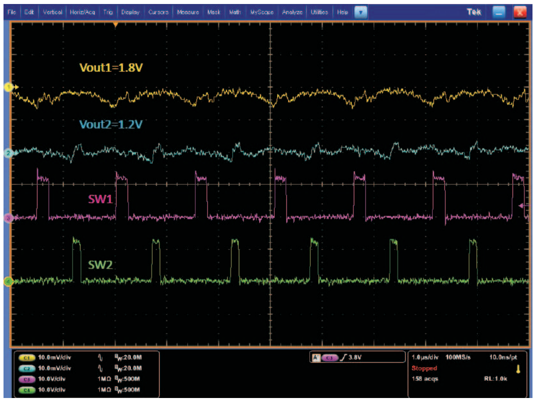


Figure 7. Buck 1 and Buck 2 in Steady State
I_{O1} = 0 A, I_{O2} = 0 A

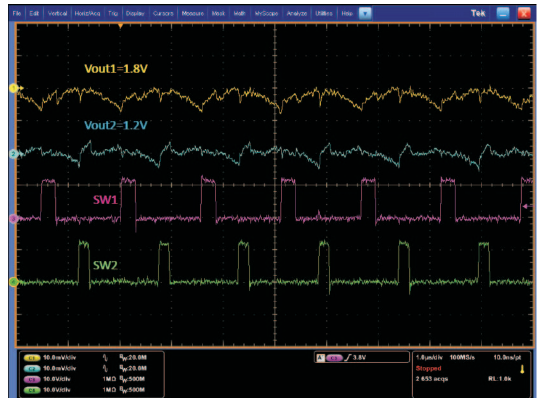


Figure 8. Buck 1 and Buck 2 in Steady State
I_{O1} = 2 A, I_{O2} = 3 A

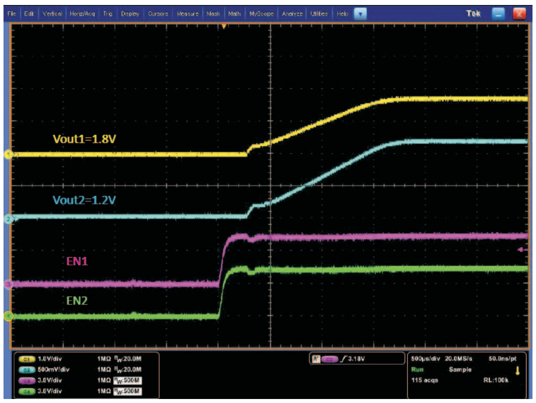


Figure 9. Startup With EN
V_{O1} = 1.8 V, V_{O2} = 1.2 V

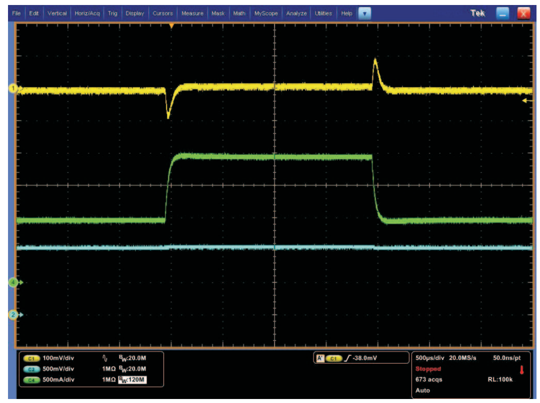


Figure 10. Buck 1 Load Transient
V_{O1} = 3.3 V, I_{O1} = 1 A - 2 A

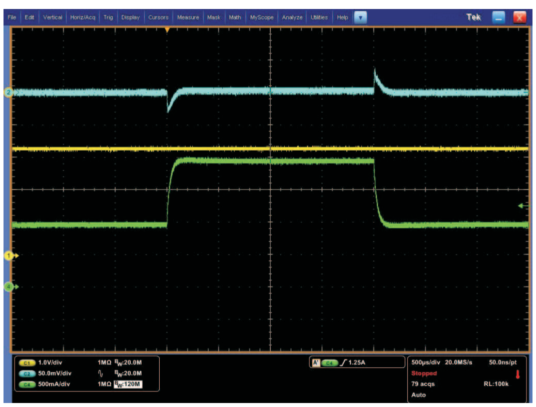


Figure 11. Buck 2 Load Transient
V_{O2} = 1 V, I_{O1} = 1 A - 2 A

Figure 12. Buck 1 and Buck 2 in PSM Mode

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 625 kHz (unless otherwise noted)

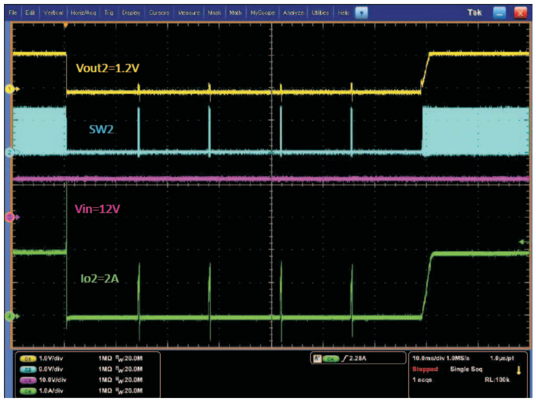


Figure 13. Buck 2 Hard Short and Recover

OVERVIEW

TPS65270 is a power management IC with two step-down buck converters. Both high-side and low-side MOSFETs are integrated to provide fully synchronous conversion with higher efficiency. TPS65270 can support 4.5-V to 16-V input supply, 2-A continuous current for Buck 1 and 3 A for Buck 2. The buck converters have an automatic PSM mode, which can improve power dissipation during light loads. Alternatively, the device implements a constant frequency mode by connecting the LOW_P pin to ground. The wide switching frequency of 300 kHz to 1.4 MHz allows for efficiency and size optimization. The switching frequency is adjustable by selecting a resistor to ground on the ROSC pin. Input ripple is reduced by 180° out-of-phase operation between Buck 1 and Buck 2.

Both buck converters have peak current mode control which simplifies the loop compensation. A traditional type II compensation network can stabilize the system and achieve fast transient response. Moreover, an optional capacitor in parallel with the upper resistor of the feedback divider provides one more zero and makes the crossover frequency over 100 kHz. Each buck converter has an individual cycle-by-cycle current limit and low side reverse current limit.

The device has a built-in LDO regulator. During a standby mode, the 6.5-V LDO can be used to drive MCU and other active loads. with this LDO, system is able to turn off the two buck converters so as to reduce the power consumption and improve the standby efficiency. Each converter has its own programmable soft start that can reduce the input inrush current. The individual Enable pins for each independent control of each output voltage and power sequence.

DETAILED DESCRIPTION

Adjustable Switching Frequency

To select the internal switching frequency connect a resistor from ROSC to ground. Figure 14 shows the required resistance for a given switching frequency.

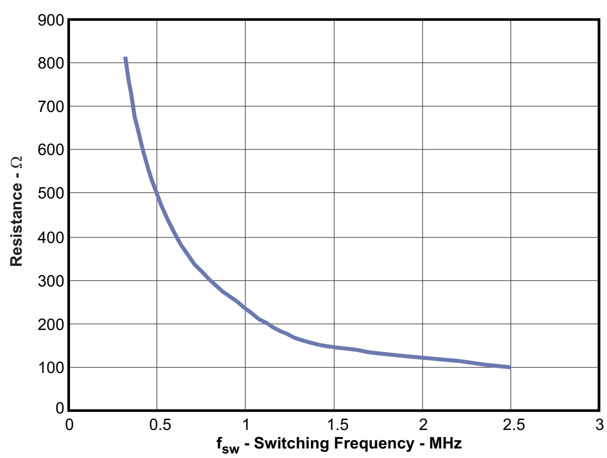


Figure 14. ROSC vs Switching Frequency

$$R_{OSC}(k\Omega) = 238 \bullet f_{SW}^{-1.05} \quad (1)$$

For operation at 800 kHz, a 300-kΩ resistor is required.

Out-of-Phase Operation

In order to reduce input ripple current, Buck 1 and Buck 2 operate 180° out-of-phase. This enables the system having less input ripple, then to lower component cost, save board space and reduce EMI.

Delayed Start-Up

If a delayed start-up is required on any of the buck converters fit a ceramic capacitor to the ENx pins. The delay added is ~1.67 ms per nF connected to the pin. Note that the EN pins have a weak 1-MΩ pull-up to the 5-V rail.

Soft Start Time

The device has an internal pull-up current source of 5 µA that charges an external slow start capacitor to implement a slow start time. Equation 2 shows how to select a slow start capacitor based on an expected slow start time. The voltage reference (V_{REF}) is 0.8 V and the slow start charge current (I_{SS}) is 5 µA. The soft start circuit requires 1 nF per 160 µs to be connected at the SS pin. An 800-µs soft-start time is implemented for all converters fitting 4.7 nF to the relevant pins.

$$T_{ss}(ms) = V_{REF}(V) \bullet \left(\frac{C_{ss}(nF)}{I_{ss}(\mu A)} \right) \quad (2)$$

Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better divider resistors. In order to improve efficiency at light load, start with 40.2 kΩ for the R1 resistor and use the Equation 3 to calculate R2.

$$R2 = R1 \cdot \left(\frac{0.8V}{V_O - 0.8V} \right) \quad (3)$$

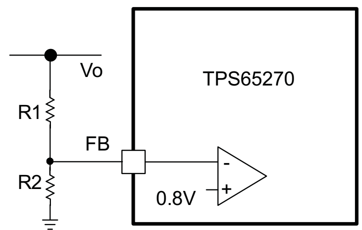


Figure 15. Voltage Divider Circuit

Input Capacitor

Use 10-µF X7R/X5R ceramic capacitors at the input of the converter inputs. These capacitors should be connected as close as physically possible to the input pins of the converters.

Bootstrap Capacitor

The device has two integrated boot regulators and requires a small ceramic capacitor between the BST and LX pin to provide the gate drive voltage for the high side MOSFET. The value of the ceramic capacitor is recommended to be 0.047 µF. A ceramic capacitor with an X7R or X5R grade dielectric is desired because of the stable characteristics over temperature and voltage.

Error Amplifier

The device has a transconductance error amplifier. The transconductance of the error amplifier is 130 µA/V during normal operation. The frequency compensation network is connected between the COMP pin and ground.

Loop Compensation

TPS65270 is a current mode control dc/dc converter. The error amplifier has 130-µA/V transconductance.

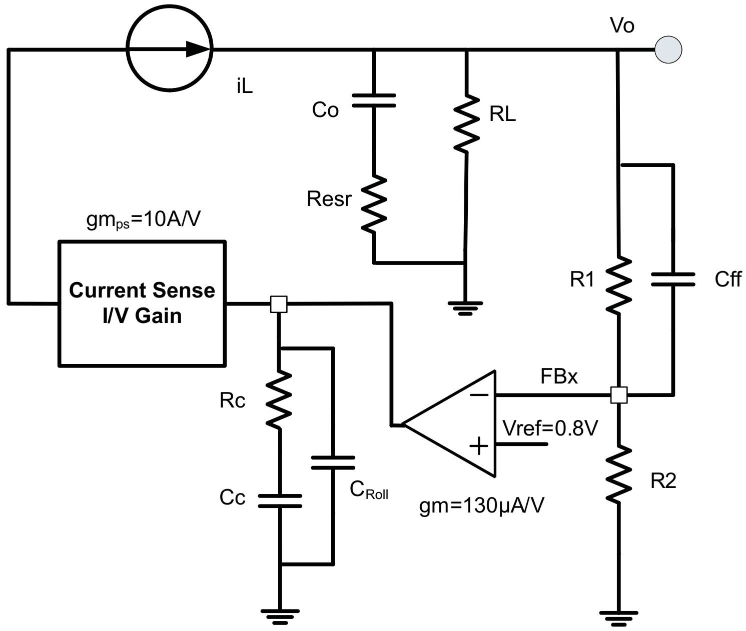


Figure 16. Loop Compensation

A typical compensation circuit could be type II (Rc and Cc) to have a phase margin between 60 and 90 degrees, or type III (Rc, Cc and Cff) to improve the converter transient response. C_{Roll} adds a high frequency pole to attenuate high-frequency noise when needed. It may also prevent noise coupling from other rails if there is possibility of cross coupling in between rails when layout is very compact.

To calculate the external compensation components follow the following steps:

	TYPE II CIRCUIT	TYPE III CIRCUIT
Select switching frequency that is appropriate for application depending on L, C sizes, output ripple, EMI concerns and etc. Switching frequencies between 500 kHz and 1 MHz give best trade off between performance and cost. When using smaller L and Cs, switching frequency can be increased. To optimize efficiency, switching frequency can be lowered.		Use type III circuit for switching frequencies higher than 500 kHz.
Select cross over frequency (fc) to be less than 1/5 to 1/10 of switching frequency.	Suggested fc = fs/10	Suggested fc = fs/10
Set and calculate R_c.	$R_C = \frac{2\pi \cdot fc \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}}$	$R_C = \frac{2\pi \cdot fc \cdot Co}{g_M \cdot gm_{ps}}$
Calculate C_c by placing a compensation zero at or before the converter dominant pole $fp = \frac{1}{C_O \cdot R_L \cdot 2\pi}$	$C_c = \frac{R_L \cdot Co}{R_c}$	$C_c = \frac{R_L \cdot Co}{R_c}$
Add C_{Roll} if needed to remove large signal coupling to high impedance COMP node. Make sure that $fp_{Roll} = \frac{1}{2 \cdot \pi \cdot R_C \cdot C_{Roll}}$ is at least twice the cross over frequency.	$C_{Roll} = \frac{\mathrm{Re}sr \cdot Co}{R_C}$	$C_{Roll} = \frac{\mathrm{Re}sr \cdot Co}{R_C}$
Calculate C_{ff} compensation zero at low frequency to boost the phase margin at the crossover frequency. Make sure that the zero frequency (fz_{ff} is smaller than soft start equivalent frequency ($1/T_{SS}$).	NA	$C_{ff} = \frac{1}{2 \cdot \pi \cdot fz_{ff} \cdot R_1}$

Slope Compensation

The device has a built-in slope compensation ramp. The slope compensation can prevent sub harmonic oscillations in peak current mode control when duty cycle becomes too large.

Over Current Protection

The current through the internal high side MOSFET is sampled and scaled through an internal pilot device during the hig time. The sampled current is compared to over current limit. If the peak inductor current exceeds the over current limit reference level, an internal over current fault counter is set to 1 and an internal flag is set. The internal power MOSFET is immediately turned off and will not be turned on again until the next switching cycle. The protection circuitry continues to monitor the current and turns off the internal MOSFET as described. If the overcurrent condition persists for four sequential clock cycles, the over-current fault counter overflows indicating an overcurrent fault condition exists. The regulator is shut down and power good goes low. If the overcurrent condition clears prior to the counter reaching four consecutive cycles, the internal flag and counter are reset. The protection circuitry attempts to recover from the overcurrent condition after waiting four soft-start cycles. The internal overcurrent flag and counter are reset. A normal soft-start cycle is attempted and normal operation continues if the fault condition has cleared. If the overcurrent fault counter overflows during soft-start, the converter shuts down and this hiccup mode operation repeats.

Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 160°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds thermal trip threshold. Once the die temperature decreases below 140°C, the device reinitiates the power up sequence. The thermal shutdown hysteresis is 20°C.

Power Dissipation

The total power dissipation inside TPS65270 should not to exceed the maximum allowable junction temperature of 125°C to maintain reliable operation. The maximum allowable power dissipation is a function of the thermal resistance of the package (R_{JA}) and ambient temperature.

To calculate the temperature inside the device under continuous loading use the following procedure.

1. Define the set voltage for each converter.
2. Define the continuous loading on each converter. Make sure do not exceed the converter maximum loading.
3. Determine from the graphs below the expected losses in watts per converter inside the device. The losses depend on the input supply, the selected switching frequency, the output voltage and the converter chosen.
4. To calculate the maximum temperature inside the IC use the following formula:

$$T_{HOT\_SPOT} = T_A + P_{DIS} \bullet \theta_{JA} \tag{4}$$

Where:

T_A is the ambient temperature

P_{DIS} is the sum of losses in all converters

θ_{JA} is the junction to ambient thermal impedance of the device and it is heavily dependant on board layout

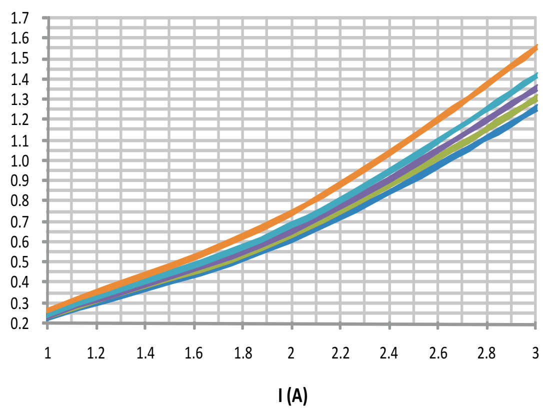


Figure 17. Buck 1
V_{IN} = 12 V, f_{SW} = 500 kHz
V_O (from top to bottom) = 5 V, 3.3 V, 2.5 V, 1.8 V, 1.2 V

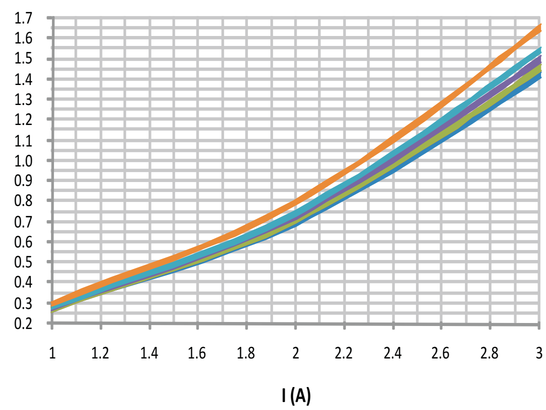


Figure 18. Buck 1
V_{IN} = 12 V, f_{SW} = 1.1 MHz
V_O (from top to bottom) = 5 V, 3.3 V, 2.5 V, 1.8 V, 1.2 V

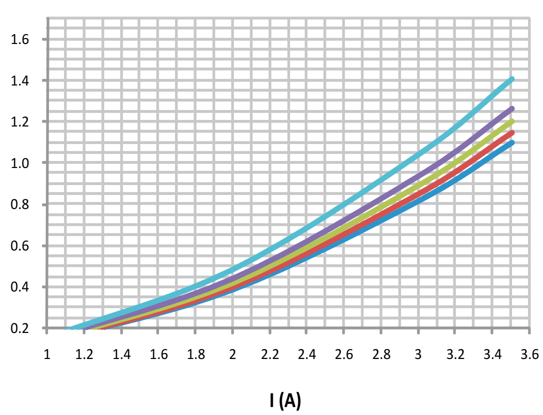


Figure 19. Buck 2
V_{IN} = 12 V, f_{SW} = 500 kHz
V_O (from top to bottom) = 5 V, 3.3 V, 2.5 V, 1.8 V, 1.2 V

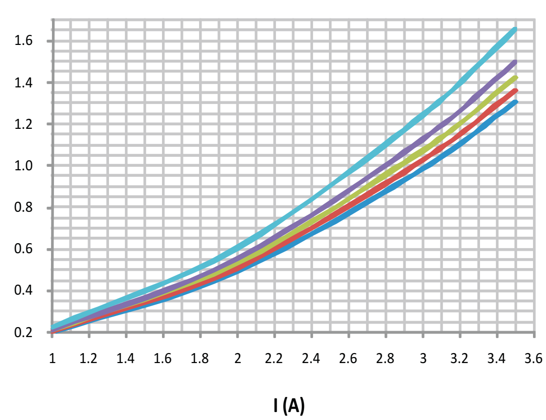


Figure 20. Buck 2
V_{IN} = 12 V, f_{SW} = 1.1 MHz
V_O (from top to bottom) = 5 V, 3.3 V, 2.5 V, 1.8 V, 1.2 V

Low Power Mode Operation

By pulling the Low_P pin high all converters will operate in pulse-skipping mode, greatly reducing the overall power consumption at light and no load conditions. When LOW_P is tied to low, all converters run in forced PWM mode.

Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 160°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds thermal trip threshold. Once the die temperature decreases below 140°C, the device reinitiates the power up sequence. The thermal shutdown hysteresis is 20°C.

Layout Recommendations

Layout is a critical portion of PMIC designs.

- Place VOUT, and LX on the top layer and an inner power plane for VIN.
- Fit also on the top layer connections for the remaining pins of the PMIC and a large top side area filled with ground.
- The top layer ground area sould be connected to the bottom ground layer(s) using vias at the input bypass capacitor, the output filter cpacitor and directly under the TPS65270 device to provide a thermal path from the Powerpad land to ground.
- The AGND pin should be tied directly to the power pad under the IC and the power pad.
- For operation at full rated load, the top side ground area together with the bottom ground plane, must provide adequate heat dissipating area.
- There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the ground connections. Since the LX connection is the switching node, the output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The output filter capacitor ground should use the same power ground trace as the VIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width.
- The compensation should be as close as possible to the COMP pins. The COMP and OSC pins are sensitive to noise so the components associated to these pins should be located as close as possible to the IC and routed with minimal lengths of trace.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS65270PWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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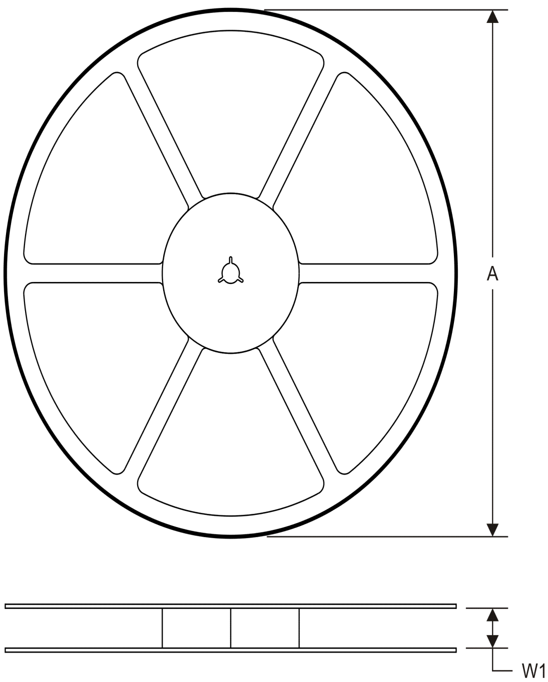
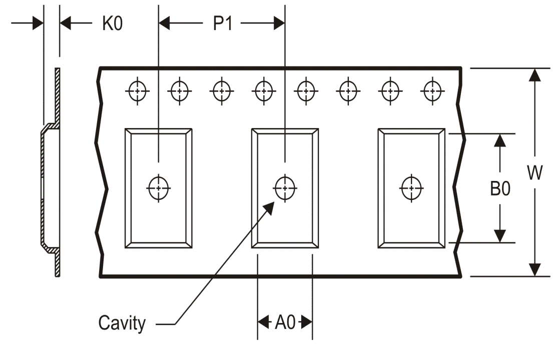
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



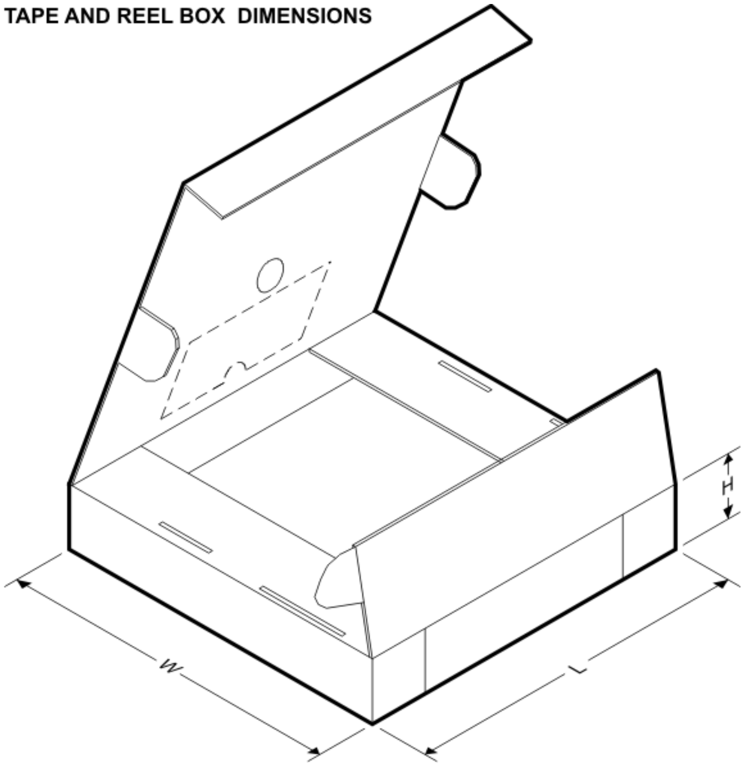
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65270PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

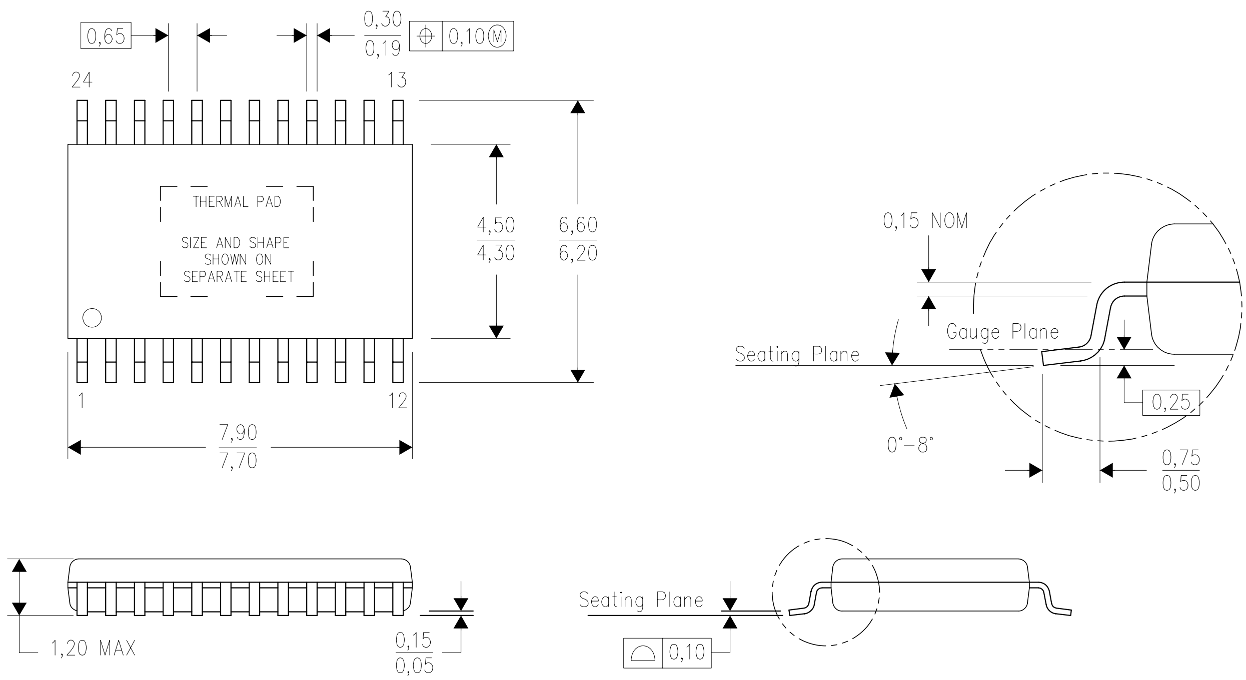
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65270PWPR	HTSSOP	PWP	24	2000	346.0	346.0	33.0

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

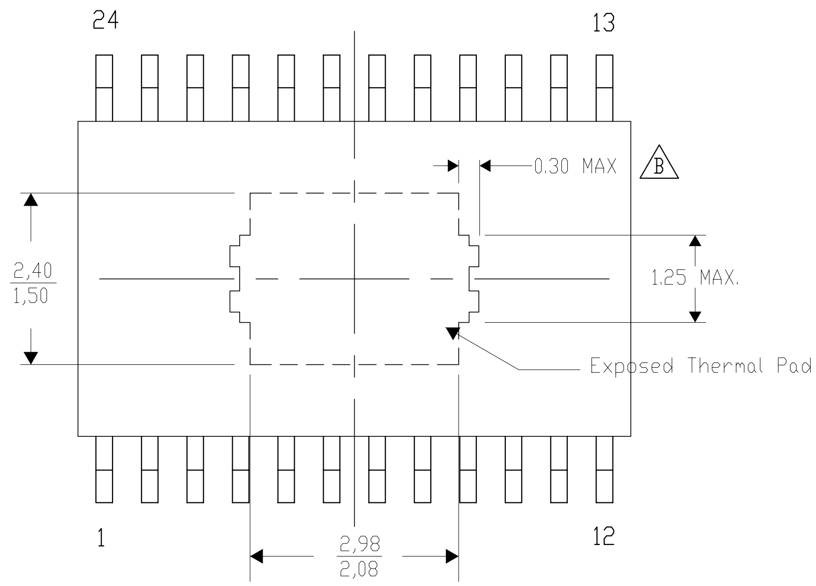
PWP (R-PDSO-G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-27/X 09/11

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments